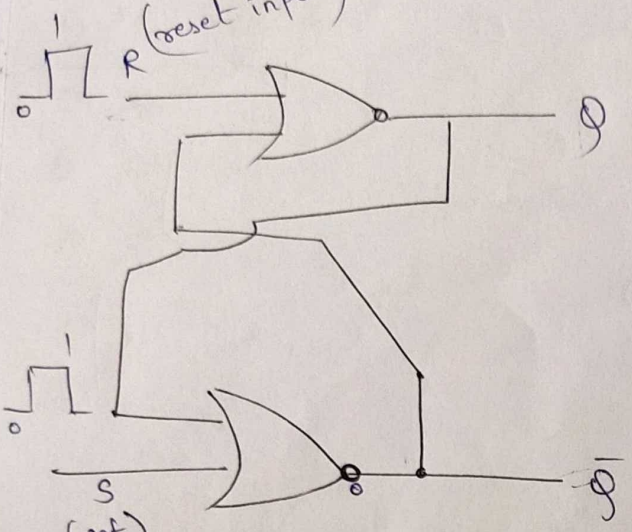
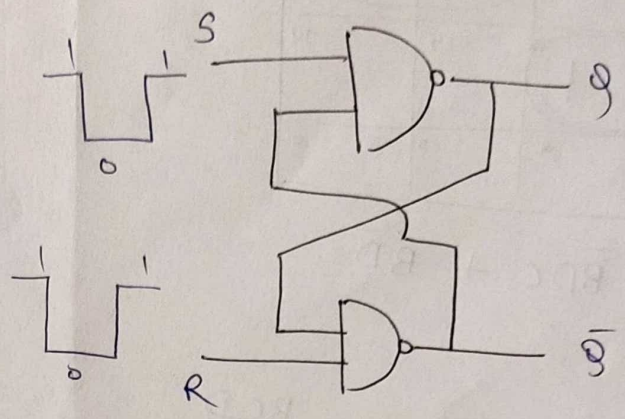
25/10/24

UNIT - 3

flip flops



using NOR gate



using NAND gate

	S	R	Q	Q'
	1	0	1	0
after → s=1; R=0	0	0	1	0
	0	1	0	1
after → s=0; R=1	0	0	0	1
	1	1	0	0

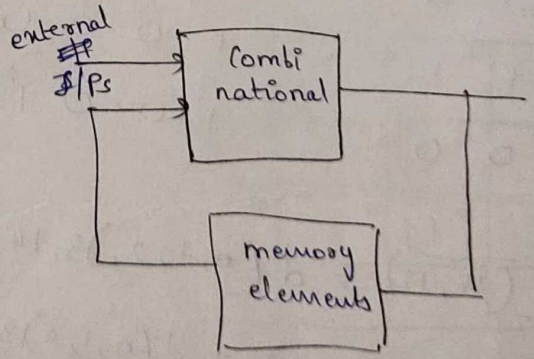
	S	R	Q	Q'
	1	0	0	1
after s=1; R=0 →	1	1	0	1
	0	1	1	0
after s=0; R=1 →	1	1	1	0
	0	0	1	1

~~Diff btw flip~~

⇒ A flip flop circuit can maintain binary information indefinitly as long as the power is delivered to the circuit until directed by an input signal to switch state

⇒ basically it can be constructed using two NAND gates (or) NOR gates with cross coupled connection from o/p of one gate ~~to~~ to I/p of other gate

This provides a feedback path



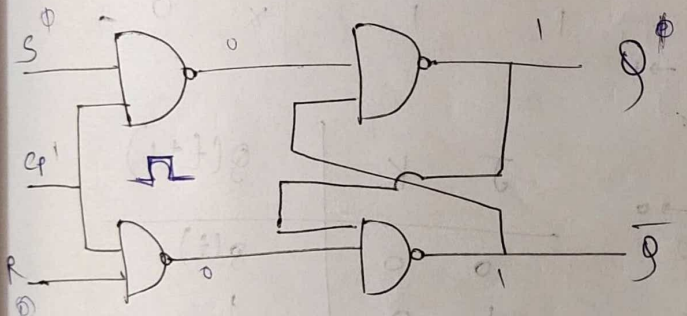
flip flop is sequential c

Latch

1) o/p changes immediately when I/p changes
2) It consumes less power because of simpler design and no clocking mechanism
3) Used in ~~more~~ mainly logicall combinational circuits
4) no clock signal, gates used
5) Assenchronous sequential circuit

flip flop

1) o/p changes only with the clock signals
2) It consums more power because of its more complex is clocking mechanisms
3) Important modules in sequential circuits
4) Clock signal applicaation is required
5) sequential ~~so~~ synchronous circuit

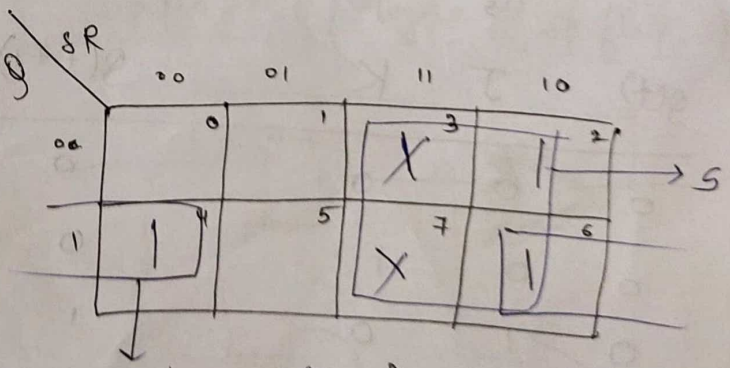


SR flip flop → Truth table

i/ps S	i/ps R	o/p Q(t+1)
0	0	Q(t) ← no change
1	0	1 ← set the o/p to 1
0	1	0 ← reset the o/p to 0
1	1	xx invalid

⇒ characteristic equation

Q(t)	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate



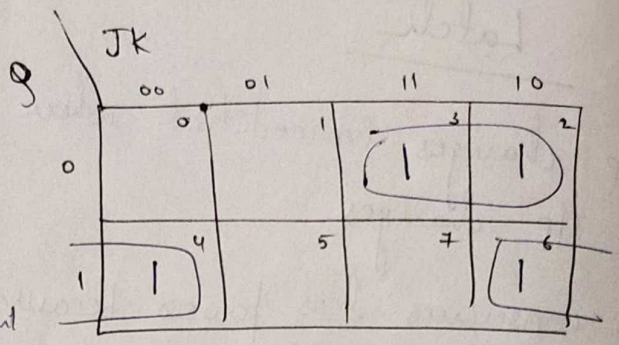
$Q(t+1) = S + R'Q$

$SR = 0$

⇒ Excitation table

Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

(S, R: complement)



$Q(t+1) = JQ' + K'Q$

characteristics equation of J-K

disadvantage Indeterminate

so modification of this JK flip flop can be used

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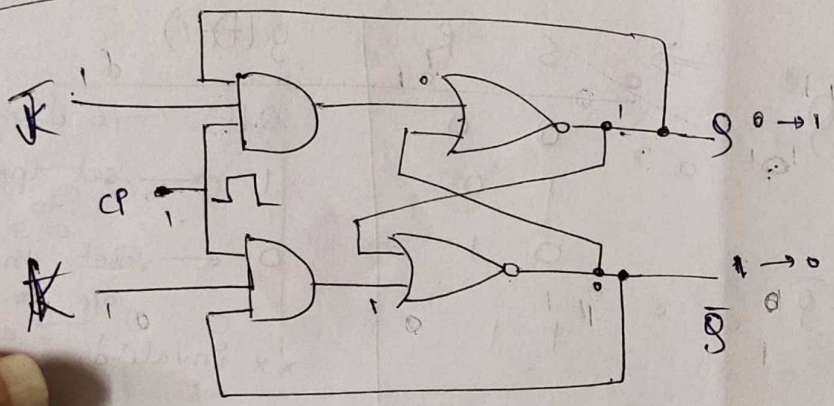
J-K flip flop



JK excitation table

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

J	K	Q(t+1)
0	0	Q(t)
1	0	1
0	1	0
1	1	Q'(t)

characteristics table →

i/p's Q(t)	J	K	o/p Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

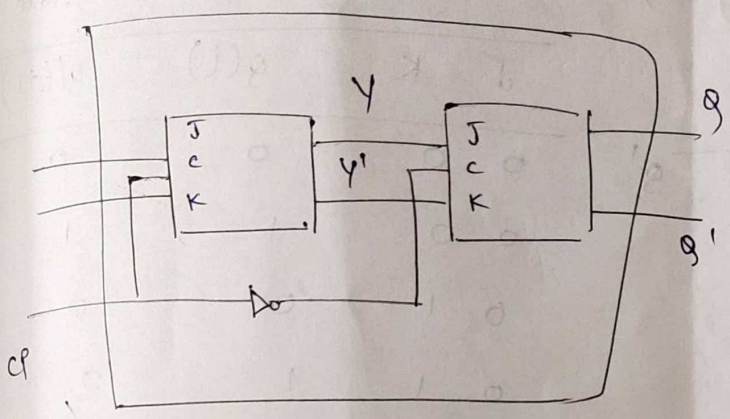
⇒ Race-around condition

for the duration of clock pulse the output will oscillate b/w 0 and 1, and at the end of clock pulse value of Q is uncertain for J = K = 1

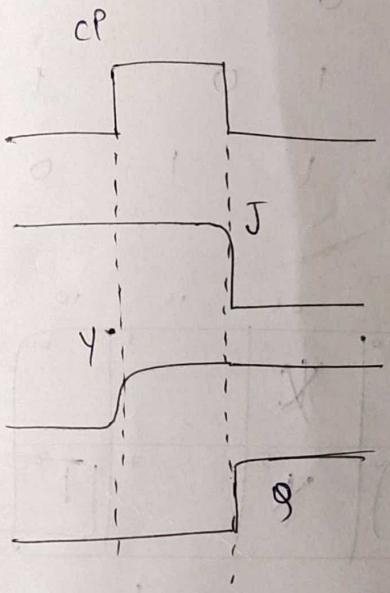
this situation is referred to as race-around condition

It can be avoided if $t_p < \Delta t$

— To avoid this situation master slave J-K flip flop can be used

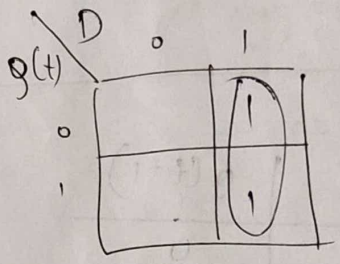


master slave JK FF



i/ps		o/p
Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

truth table



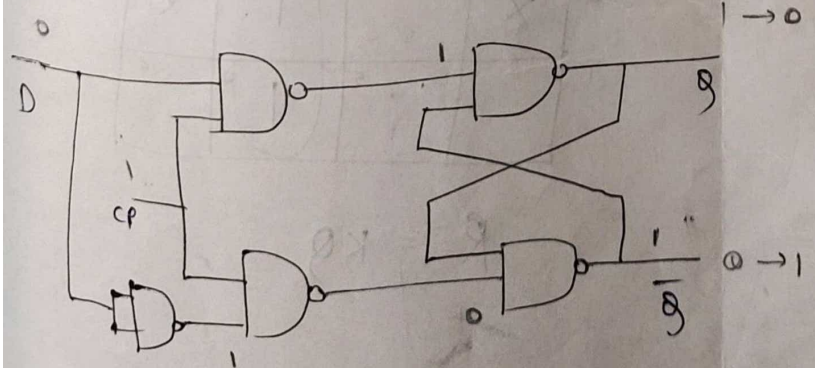
$Q(t+1) = D$

characteristic equation

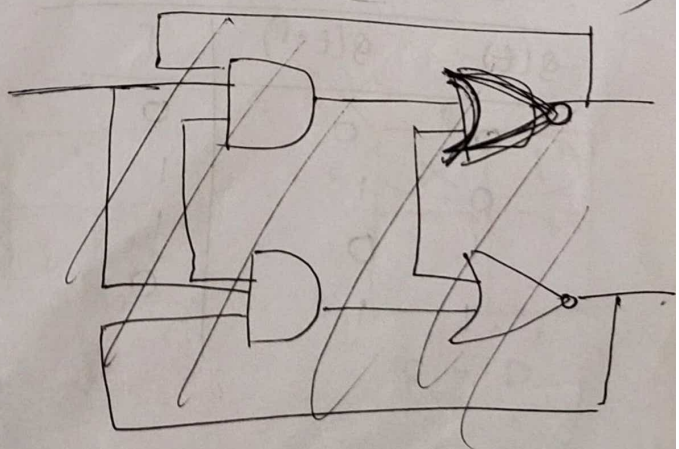
Excitation table

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

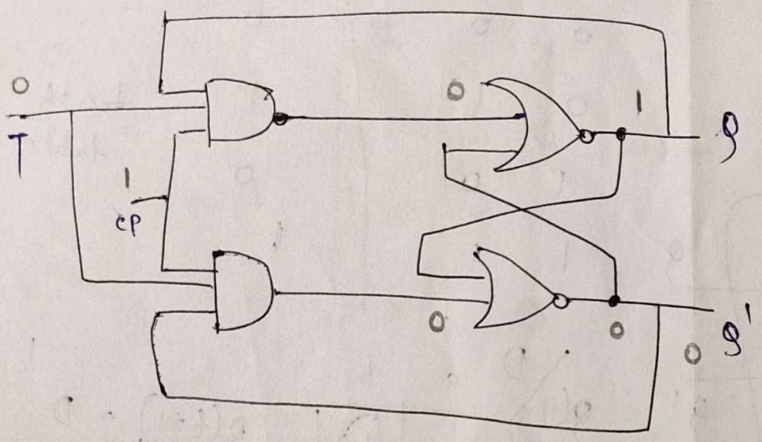
D-flip flop (Data flip flop)



T flip flop (Toggle flip flop)

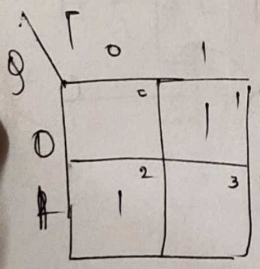


T flip flop



Q(t)	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

truth table



$Q(t+1) = TQ' + T'Q$

characteristic eq

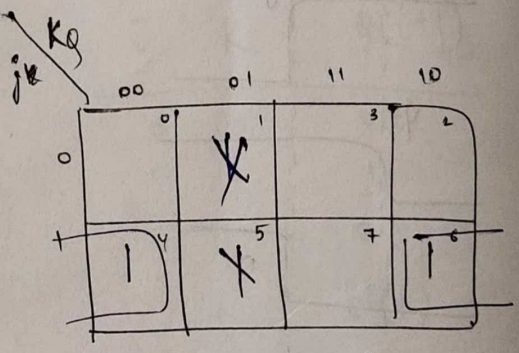
Excitation table

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

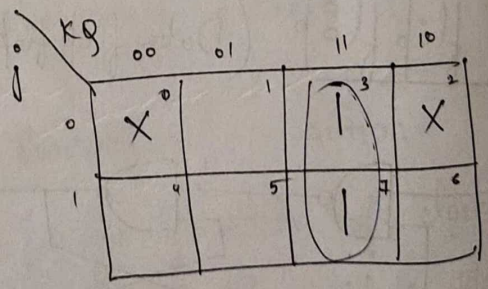
flip-flop conversions (9)

SR FF → JK FF

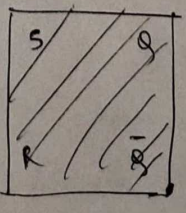
J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



$S = JQ'$



$R = KQ$



JK FF ⟶ SR FF

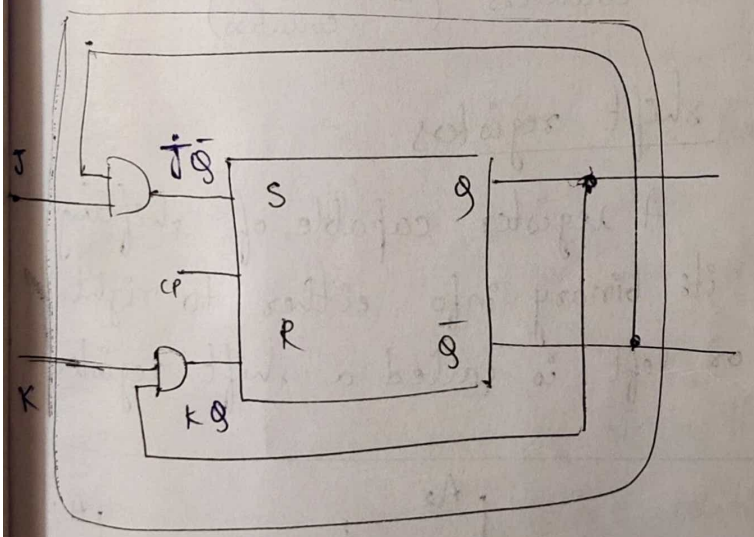
i/ps	Present state	next state	FF i/ps	
S	R	Q(t)	Q(t+1)	J	K
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

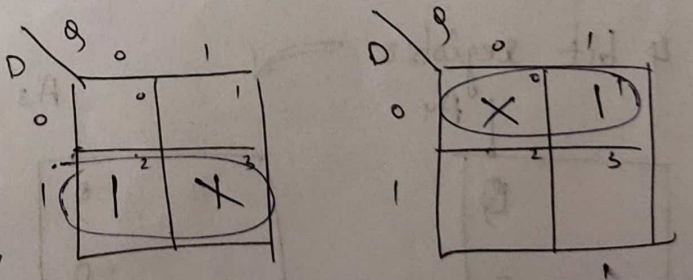
any other ⟶ SR is not recomended as invalid

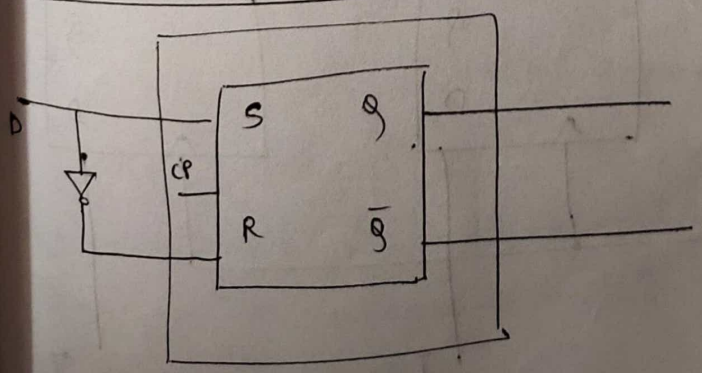
FF i/ps	
S	R
0	X
X	0
0	X
0	1
1	0
X	0
1	0
0	1

SR ⟶ D

i/ps			
D	Q(t)	Q(t+1)	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0







Assignment

Any two flip flop conversions

T ⟶ D

D ⟶ T